13. (New) A semiconductor device comprising:

a substrate;

a thin film transistor provided over said substrate; and

a metal layer provided over said substrate and being in direct contact with a gate electrode of said thin film transistor to form an interconnect comprising said metal layer.

14. (New) A semiconductor device comprising:

a substrate;

a thin film transistor provided over said substrate; and

a metal layer provided over said substrate and being in direct contact with a gate electrode of said thin film transistor and being connected with one of source and drain regions of said thin film transistor.

15. (New) A semiconductor device comprising:

a substrate;

a thin film transistor provided over said substrate; and an interconnect provided over said substrate and being in direct contact with a gate electrode of said thin film transistor,

wherein said interconnect comprises a refractory metal layer and an aluminum layer.

16. (New) A semiconductor device comprising:

a substrate;

a thin film transistor provided over said substrate; and an interconnect provided over said substrate and being in direct contact with a gate electrode of said thin film transistor,

wherein said interconnect comprises an aluminum layer and a metal layer which comprises an element selected from the group consisting of titanium, molybdenum, tungsten, platinum, chromium and cobalt.

17. (New) A semiconductor device comprising:

a substrate;

a thin film transistor provided over said substrate; and a metal layer provided over said substrate and being in direct contact with a gate electrode of said thin film transistor and being in direct contact with one of source and drain regions of another thin film transistor to form an interconnect comprising said metal layer connected between said gate electrode and said one of source and drain regions of another thin film transistor.

18. (New) A semiconductor device comprising:

a substrate;

a thin film transistor provided over said substrate; and an interconnect provided over said substrate and being in direct contact with a gate electrode of said thin film transistor and being connected with one of source and drain regions of said thin film transistor,

wherein said interconnect comprises a refractory metal layer and an aluminum layer.

19. (New) The device of claim 13 wherein said metal layer is connected with said gate electrode through no contact hole.

20. (New) The device of claim 13 wherein said metal layer has a part provided on a same surface as a semiconductor island of said thin film transistor which comprises a source region, a drain region, and a channel region provided between said source region and said drain region.

21. (New) The device of claim 13 wherein said metal layer has a part provided in a same plane as a semiconductor island of said thin film transistor which comprises a source

region, a drain region, and a channel region provided between said source region and said drain region.

22. (New) The device of claim 13 wherein at least a part of said gate electrode comprises a doped polycrystalline silicon film.

23. (New) The device of claim 13 further comprising an interlayer dielectric comprising a material selected from the group consisting of silicon nitride and silicon oxide provided over said metal layer and said thin film transistor.

24. (New) The device of claim 14 wherein said metal layer is connected with said gate electrode through no contact hole.

25. (New) The device of claim 14 wherein said metal layer has a part provided on a same surface as a semiconductor island of said thin film transistor which comprises said source and drain regions, and a channel region provided between said source and drain regions.

26. (New) The device of claim 14 wherein said metal layer has a part provided in a same plane as a semiconductor

island of said thin film transistor which comprises said source and drain regions, and a channel region provided between said source and drain regions.

27. (New) The device of claim 14 wherein at least a part of said gate electrode comprises a doped polycrystalline silicon film.

28. (New) The device of claim 14 further comprising an interlayer dielectric comprising a material selected from the group consisting of silicon nitride and silicon oxide provided over said metal layer and said thin film transistor.

29. (New) The device of claim 15 wherein said aluminum layer is provided on said refractory metal layer.

30. (New) The device of claim 15 wherein said interconnect is connected with said gate electrode through no contact hole.

31. (New) The device of claim 15 wherein said interconnect has a part provided on a same surface as a semiconductor island of said thin film transistor which

comprises a source region, a drain region, and a channel region provided between said source region and said drain region.

32. (New) The device of claim 15 wherein said interconnect has a part provided in a same plane as a semiconductor island of said thin film transistor which comprises a source region, a drain region, and a channel region provided between said source region and said drain region.

33. (New) The device of claim 15 wherein at least a part of said gate electrode comprises a doped polycrystalline silicon film.

34. (New) The device of claim 15 wherein said aluminum layer has a smaller resistivity than said refractory metal layer.

35. (New) The device of claim 15 further comprising an interlayer dielectric comprising a material selected from the group consisting of silicon nitride and silicon oxide provided over said interconnect and said thin film transistor.

36. (New) The device of claim 15 wherein said aluminum layer has a thickness between 6000 to 10000 A.

37. (New) The device of claim 16 wherein said aluminum layer is provided on said metal layer.

38. (New) The device of claim 16 wherein said interconnect is connected with said gate electrode through no contact hole.

39. (New) The device of claim 16 wherein said interconnect has a part provided on a same surface as a semiconductor island of said thin film transistor which comprises a source region, a drain region, and a channel region provided between said source region and said drain region.

40. (New) The device of claim 16 wherein said interconnect has a part provided in a same plane as a semiconductor island of said thin film transistor which comprises a source region, a drain region, and a channel region provided between said source region and said drain region.

41. (New) The device of claim 16 wherein at least a part of said gate electrode comprises a doped polycrystalline silicon film.

42. (New) The device of claim 16 wherein said aluminum layer has a smaller resistivity than said metal layer.

43. (New) The device of claim 16 further comprising an interlayer dielectric comprising a material selected from the group consisting of silicon nitride and silicon oxide provided over said interconnect and said thin film transistor.

44. (New) The device of claim 16 wherein said aluminum layer has a thickness of 6000 to 10000 A.

45. (New) The device of claim 17 wherein said metal layer is connected with said gate electrode through no contact hole.

46. (New) The device of claim 17 wherein at least a part of said gate electrode comprises a doped polycrystalline silicon film.

47. (New) The device of claim 17 further comprising an interlayer dielectric comprising a material selected from the group consisting of silicon nitride and silicon oxide provided over said metal layer.

48. (New) The device of claim 18 wherein said aluminum layer is provided on said refractory metal layer.

49. (New) The device of claim 18 wherein said interconnect is connected with said gate electrode through no contact hole.

50. (New) The device of claim 18 wherein said interconnect has a part provided on a same surface as a semiconductor island of said thin film transistor which comprises said source and drain regions, and a channel region provided between said source and drain regions.

51. (New) The device of claim 18 wherein said interconnect has a part provided in a same plane as a semiconductor island of said thin film transistor which comprises said source and drain regions, and a channel region provided between said source and drain regions.

52. (New) The device of claim 18 wherein at least a part of said gate electrode comprises a doped polycrystalline silicon film.